Arguments/Remarks:

Applicants thank Examiner Chung again for her careful examination of this application and the clear explanation of the claim rejections; and for conditionally allowing claims 3 and 16.

In response to the Office Action of Nov. 1, 2006, applicants:

a. amend claim 2 to incorporate all claim elements from claim 1 into claim 2 and rewrite claim 2 in independent form, the scope of claim 2 does not change;

b. amend claim 26, incorporating the claim elements in claim 25 into claim 26 and rewrite claim 26 in independent form, the scope of claim 26 does not change;

c. cancel claim 1 and claim 25 from this examination;

d. amend claims 4, 5, and 6 to depend properly from claim 2.

Claim 2

As amended, claim 2 describes a method of testing at least one mixed signal semiconductor device. The method requires a single processor to perform the testing steps of a mixed signal semiconductor device including: executing a first test, preparing execution of a second test while executing the first test, processing test data from the first test, and executing the second test concurrently with the processing of the test data.

Claim 2 stands rejected under 35 U.S.C. 102(e) as being anticipated by Sugamori.[1] Applicants respectfully submit that, because the Sugamori patent does not disclose all the claim elements in claim 2, it cannot anticipate claim 2.

The Office Action suggests that Sugamori discloses the mixed signal semiconductor testing is performed by a single processor (67).[2] There are two facts that contradict this suggestion:

[1] U.S. 6,536,006 issued Mar. 18, 2003 from an application filed Nov. 12, 1999 by Shigeru Sugamori.

First, at least two processors are in the Sugamori test system – element 41, the Tester Controller, and element 67, the Process.[3]

> In the test system of FIG. 4, the plurality of event tester boards 43 are controlled by a tester controller 41, which is a host computer of the test system, through a system bus 64.[4]

> The processor 67 is provided, for example, in each event tester board, and controls the operations in the event tester board including generation of events (test patterns), evaluation of output signals from the device under test, and acquisition of failure data. The processor 67 can be provided at each tester board or every several tester boards.[5]

It is therefore clear that Sugamori teaches a test system that has a host computer, which necessarily has at least one processor, and a processor associated with each "event tester board" to control the operations in the tester board.

In a later paragraph, Sugamori does suggest that the control functions be made by the tester controller itself:

> Further, the processor 67 may not always necessary be provided in the event tester board, but the same control functions can be made directly by the tester controller 41 to the event tester boards.[6]

But there is no disclosure in the Sugamori patent as how this can be accomplished.

Second, the processors in the Sugamori patent do not perform the multiple tasks required in claim 1 in the required fashion. In particular, they do not prepare execution of a second test while executing the first test, process test data from the first test, and executing the second test concurrently with the processing of the test data. As clearly stated in the paragraph cited in the Office Action, the invention in the Sugamori patent is that the start and end timings of the tests can be set and the tests performed independently:

---

[2] The Office Action of Nov. 1, 2006, page 3.
[3] See, Sugamori, supra, Fig. 4.
[4] Id. col. 7, lines 56 through 58.
[5] Id. col. 8, lines 50 through 56.
[6] Id. col. 8, lines 56 through 60.

> As in the foregoing, in the event based test system, each of the test pins or each group of test pins can independently perform a test operation from the other. Consequently, in the case where a plurality of different kinds of test have to be performed, such as in testing the mixed signal device under test which includes an analog signal and a digital signal, such different kinds of test can be conducted in parallel at the same time. Further, start and end timings of such different kinds of test can be independently established.[7]

Fig. 9B depicts a logic test, an A/D test, and a D/A test starting at the same time with the computation times of the two tests overlapping. In no occasions does the Sugamori patent disclose the steps required in claim 2.

Because the Sugamori patent does not disclose all the claim elements in claim 2, applicants respectfully submit that it does not anticipate claim 2 and therefore claim 2 stands patentable over the Sugamori patent.

Claim 12

Claim 12 describes an apparatus of which one component is a processor that is configured to perform the following tasks:

a. execute a first test for the at least one mixed signal semiconductor device;

b. prepare execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

c. process test data resulting from the first test; and

d. execute the second test concurrently with the processing of the test data.

Claim 12 also stands rejected under 35 U.S.C. 102(e) as being anticipated by Sugamori. The Office Action suggests that element 67 of the Sugamori patent stands for the process and it performs the tasks as required in claim 12.[8] The Office Action cites two paragraphs from the Sugamori for support:

[7] Id. col. 9, line 66 through col. 10, line 8.
[8] The Office Action, supra, page 2 bridging page 3.

> As in the foregoing, in the event based test system, each of the test pins or each group of test pins can independently perform a test operation from the other. Consequently, in the case where a plurality of different kinds of test have to be performed, such as in testing the mixed signal device under test which includes an analog signal and a digital signal, such different kinds of test can be conducted in parallel at the same time. Further, start and end timings of such different kinds of test can be independently established.[9]
>
> As has been foregoing, in the event based semiconductor test system of the present invention, each test pin can operate independently from the other test pins. Thus, by assigning groups of test pins to different devices or blocks under test, two or more different devices or blocks can be tested at the same time. Therefore, according to the semiconductor test system of the present invention, an analog circuit and a digital circuit in a mixed signal device can be tested in parallel at the same time.
>
> As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, the rate signal showing the start timing of each test cycle or the pattern generator which operates in synchronism with the rate signal used in the conventional technology are no longer necessary. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.[10]

Again, Sugamori discloses a test system that is capable of conducting different kinds of tests in parallel at the same time and the multiple test pins are capable of operating independently from one another; but it does not disclose a single process that performs all the required tasks in claim 12, and it does not disclose performing the specific tasks in a fashion required in claim 12. Therefore, applicants respectfully submit that claim 12 cannot be anticipated by the Sugamori patent and it stands patentable over the reference.

[9] Id.
[10] Id. col. 11, line 66 to col. 12, line 22.

Claim 26

Claim 26 is amended to incorporate all the claim elements in claim 25 so claim 26 is written in independent form as amended.

The Office Action rejects claim 26 on the same ground as it rejects claim 7 through 11.[11] In rejecting claims 7 through 11, the Office Action reasons that even though Sugamori does not disclose wherein the interpreted software language is Interactive Test Pascal, it nevertheless would have been obvious to a person of ordinary skill in the art.

Claim 26 in independent form, describes a computer program that has a set of instructions configured to enable a mixed signal semiconductor device test system to do the following on a single processor:

a. execute a first test for at least one mixed signal semiconductor device;

b. prepare execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

c. process test data resulting from the first test; and

d. execute the second test concurrently with the processing of the test data.

Applicants respectfully submit that claim 26 stands patentable over the Sugamori patent not because of the language in which it is written, but because the Sugamori patent fails to disclose all the claim elements in claim 26 for the reason presented above regarding claims 2 and 12.

Regarding claims 4 through 11, they properly depend from patentable claim 2 and stand patentable at least by virtue of their dependence.

Regarding claims 13 and 14, they properly depend from patentable claim 12 and stand patentable at least by virtue of their dependence.

[11] The Office Action, supra, page 4.

Regarding claim 15, applicants respectfully submit that because the Office Action rejects this claim on the same ground as it does claim 2, the reason presented above regarding claim 2 being patentable applies to claim 15 – the Sugamori patent does not disclose a single processor performing the tasks in the fashion as required in claim 15, claim 15 stands patentable over the Sugamori patent.

Regarding claims 17 through 24, they properly depend from claim 15 and claim 12, and stand patentable at least by virtue of their dependence.

Regarding claim 27, it has similar claim elements as in claim 2 and 16. Applicants respectfully submit that claim 27 stands patentable at least for the same reason that claims 2 and 16 being patentable.

Regarding claim 28 through 34, they properly depend from claim 26 and stand patentable at least by virtue of their dependence.

In light of the amendments and the reasons presented above, applicants respectfully request further examination of this application and timely allowance of all pending claims.

Respectfully submitted,
/Yingsheng Tung/

Yingsheng Tung
Reg. No. 52,305
Attorney for Applicants

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5355